SILICONOVA

Solving Hardest Engineering Problem

SILICONOVA LIMITED
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Begum Rokeya Sharani, Dhaka 1216, Bangladesh

Executive Team

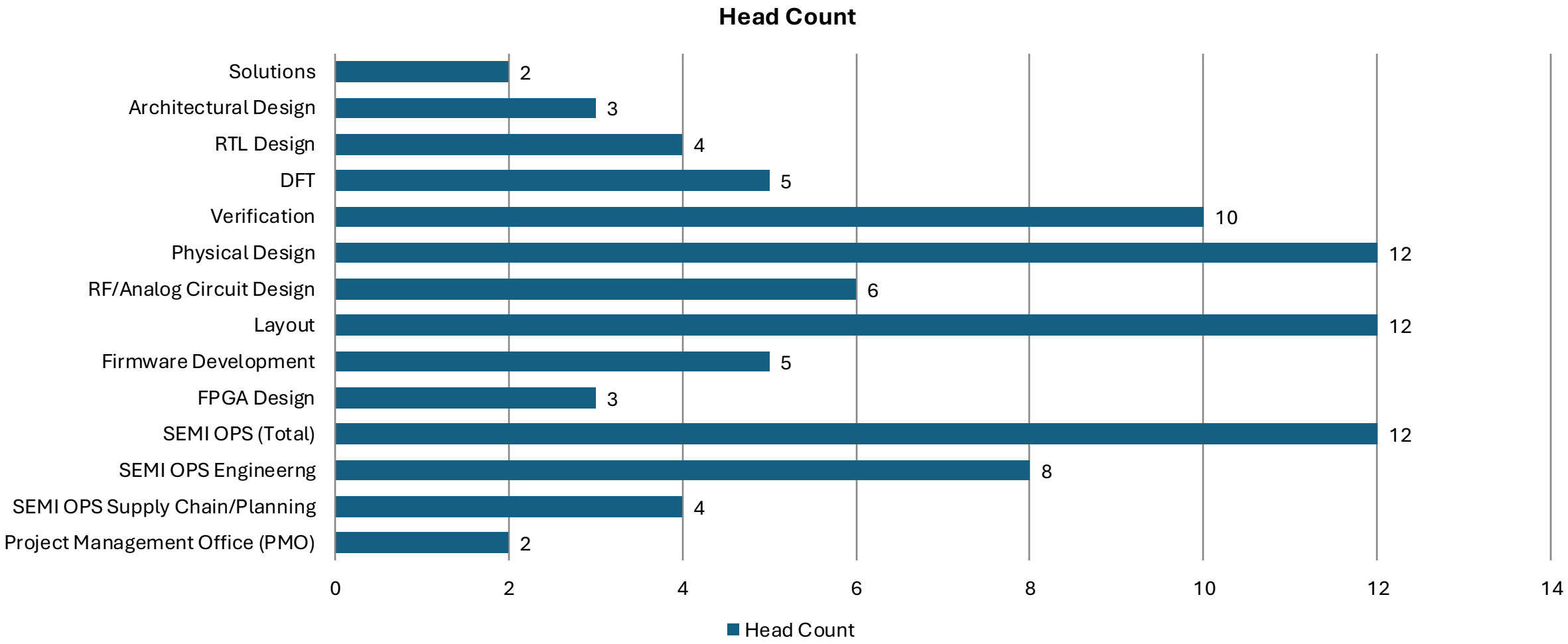
Sirajul Khan
Founder/CEO

Shafil Hossain
Co-Founder / Director

Mozibul Haque
Chairman

Rukunuzzaman Inam
Director

Engineering Resources



CUSTOMERS

In Progress

In Progress

CUSTOMERS

40% 30% 20%

North American Market

- PnR Project
- Analog Layout
- IC Package Design

Europe

- DV, DFT
- Analog Circuit Design

South East Asia

- Design Verification
- PnR
- Analog Layout

OUR SERVICES

Design Verification

•Feature Extraction From Specification.
•Develop Test Plan Which Includes Stimulus Generation Plan, Functionality Checking And Coverage Modeling.
•Review The Test Plan With Design Team.
•Develop Testbench Environment And Other Components For Verifying Each Block In Design.
•Create Necessary Test Cases To Ensure Desired Functionality Of Each Block.
•Run Regression Tests At Block Level And Report Bugs In RTL.
•Create Directed And Randomized Test Cases To Check Corner Cases In Design.

Physical Design

•Multiple Voltage Design
•Complex Clocking Scheme: Clock Mesh, Multisource
•Flat, Virtual Flat, Hierarchical, Chip-Assembly Flow
•Placement & Routing
•Physical Verification
•Parasitic Extraction
•Static Timing Analysis
•Advanced STA (MMMC, AOCV, POCV)
•Power Verification
•Formal Verification
•IR/EM Analysis
•ESD And Reliability Analysis

OUR DFT SERVICES

Tessent testcompress, MBIST, BISt, JTAG, IJTAG, Synopsys DC, EV, VCS< Synthesis , Cadence Genus, Modus/ET, xcelium/irun

Siemens (Mentors), Synopsys, Cadence

Architecture	Scan Insertion	ATPG/LBIST	MBIST	DFT Verification	MISC
DFT Specification/ SoC DFT Strategy	Flat Scan Implementation	Design Rule Checks (DRC) Analysis	MBIST insertion hook up	Non-Timing Simulation	Work with ATE team/ATE Debug Support
Hierarchical EDT Implementation	Hierarchical Scan Implementation	Chain Training	Memory Grouping for Optimum TTR	SDF Annotated/ Timing Simulation	Failure Analysis Diagnosis
Modular Scan Implementation	Test Wrapper (Incest/ Extest) Insertion	Test coverage improvements	MBIST Verification	Scan VCD Generation for test Power analysis	Scan VCD Generation for test Power analysis Yield Improvement (Vmin Search)
Low Power Scan	Test mode constraints development	Test point analysis	Memory repair		Tests time reduction
Low Pin Count Test	Conformal IPV	Production Pattern Development			Higher Multisite Test (4x, 16x)
		Pattern Finishing			

PD Team Expertise

Synthesis

- **Low Power Synthesis**

Optimization of RTL to meet power budgets through clock gating, multi-voltage design, and power-aware logic restructuring.

- **Physical synthesis**

Timing, area, and power optimization of placed netlists using physical synthesis tools.

- **Library Configuration**

Characterization and configuration of standard cell, I/O, memory compilers for accurate library data.

- **MMMC Configuration**

Configured MMMC for 50+ number of scenarios with automotive grade pdf

- **Logic configuration**

Technology mapping and optimization of RTL into gate-level netlists targeting timing, area, and power.

- **Debugging**

Expertise at solving RTL,SDC and PDK issues

- **Tools**

Genus, DC , DCNXT

Place & Route

- **Floor planning**

Adept in top level floor planning and multiple macros placement.

- **Power Planning**

Expertise at top level robust and low node's power planning

- **Placement:**

Placement of standard cells and IP blocks based on routing layer consideration, boundary optimization

- **Clock Tree Synthesis**

Expertise in do the CTS according to meeting the top level criteria and meeting the ndr rule and protecting the critical net using shielding.

- **Routing**

Proficient at solving problems in lower node technology such as congestion, analog macro routing, custom routing.

- **Tools**

Innovus, ICC2, Fusion compiler

Signoff

- **Timing Signoff & ECO**

Using signoff-accurate STA tools for final timing validation. Ensuring timing closure meets constraints with high accuracy. Develop ECO and ECO flow between same and different tool vendors

- **Parasitic Extraction**

creating accurate RLC models to capture wire parasitics; proper setup of tools like StarRC & Quantus RC.

- **DRC**

Detailed design and Antenna rule checking to avoid gate oxide breakdown during manufacturing .

- **LVS**

Final layout vs schematic checking to ensure correctness between layout and netlist.

- **Power Signoff**

Accurate analysis of switching, internal, leakage power. Validate power meets budget. Analyze the IR Drop and potential PG grid issues

- **Tools**

Primetime, Primetime ECO, Tempus, Tempus ECO, StarRC, Quantus, CalibreDRC, CalibreLVS, Voltus, Redhawk, PVS, ICB

Technology Node: Samsung 8, 14nm,TSMC 7, 28, 40nm, GF 12nm, 28nm HPCP

OUR SERVICES

Custom IC Design

- Architecture Planning
- System Level Modeling
- Circuit Design And Simulation
- Block And Full Chip Layout
- Physical Verification
- Parasitic Extraction
- Post Layout Simulation
- GDSII Release

Circuit Design

- High-Speed IO Design
- IO Libraries
- Power Management Units
- Low Power Custom Circuit Design
- Custom SRAM/DRAM/TCAM Design
- PLLs, DLLs & Oscillators
- DACs And ADCs
- IP Conversion: New Process Nodes & Technologies
- Switching And Linear Regulators

IC Layout

- Standard Library Cells
- Memory Cells
- I/O Circuits
- ADC And DAC
- PLL
- Band Gap Reference
- Analog And Digital Layout Design
- RF High frequency Circuit Layout

Analog and Mixed Signal Capabilities

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Design Skills

- Cadence Tools: Virtuoso & Spectre.
- Mentor Graphics Tools: Calibre & Assura LVS and DRC.
- Layout Design Tools: Virtuoso (Layout L and Layout XL)
- Synopsys Tools: Hspice.
- Proficient in HSpice netlisting and simulation.
- Proficient in LTSpice circuit design and simulation.
- Knowledgeable about Verilog.
- Knowledgeable about ASIC Design Flow.

Operational Amplifier Full Chip Design

Process Node: 22nm & 90nm

- Completed an Industry Standard Data Sheet with design specifications and Test Bench simulation results such as Input Offset Voltage, PSRR, CMRR, UGBW, ICMR, Input offset current, Input bias current, Gain Margin, Phase Margin, SR etc.
- Designed the corresponding Layout of the op-amp and verified using Calibre DRC & LVS.

TECHNOLOGY NOD

- TSMC- 7nm, 16nm FinFET and 22nm
- GF- 14nm FinFET, 22nm FDX and 180nm
- INTEL- 10nm and 14nm FinFET
- Samsung- 10nm, 14nm FinFET
- UMC- 40nm and 45nm
- Cypress- 180nm BCD

Folded Cascode Operational Amplifier Design

Process Node: 180nm & 90nm

- Current Summing Stage design
- Differential Pair Design
- Integrating Class-AB amplifier stage.
- Investigate and Design Different Biasing Architecture

Phase Locked Loop (PLL) Design

Process Node: 90nm

- Designed a Voltage Controlled Oscillator (VCO)
- Designed a Charge Pump circuit, a Phase Detector circuit and a Frequency Divider circuit for the feedback loop.

Design & Porting

- Requirement & Feasibility Analysis
- Modeling & Mixed Signal Verification
- Circuit Design, Simulation and Analysis
- Block & Full chip Custom Design
- Pre & Post Layout Simulation
- Parasitic Extraction
- GDSIl sign off
- Silicon Evaluation

Band Gap Reference (BGR) Circuit

Design Process Node: 22nm & 90nm

- For a bipolar 2.5V supply voltage, obtained a output voltage of -60.54mV
- Obtained a 2.532mV of output voltage variation for -40°C to +125°C temperature variation.
- Designed BGR without comparator and with comparator.

Package Engineering Capability

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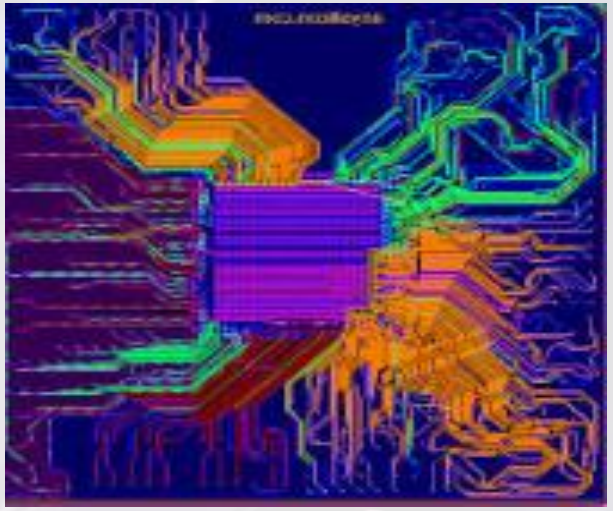
Die-Package-System Co-Design & Optimization for High Volume Manufacturing

IP Bump Optimization

- New IP Block Package Trial Routing before finalizing
- Existing IP Block improvement on performance or package cost reduction.
- RDL / bump placement for all digital areas owned by package engineer for Connectivity & Olympic custom ASICs

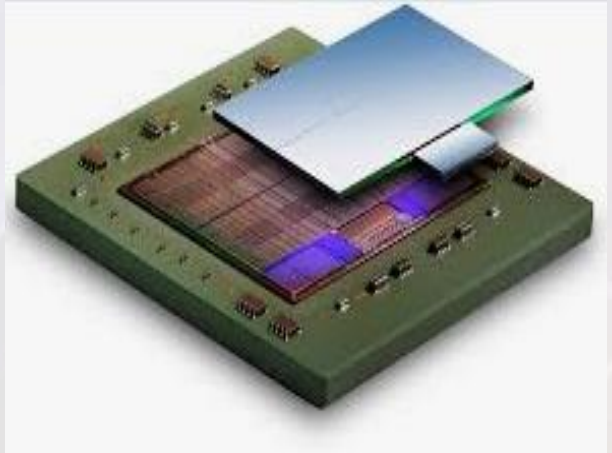


Die Floor Plan Optimization

- Verify die floor plan and IP block placement by package trial routing from die pad to package pin
- Digital signal design optimization with different package type / substrate layer count
- Chip core power / ground optimization

BGA Ballmap Optimization

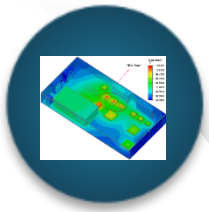
- BGA ball map assignment with to optimize performance, optimize and cost



Substrate /Package Design

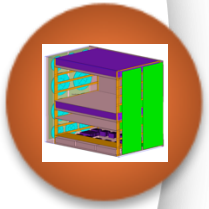
- Performance, Reliability & Cost driven Package/Substrate design supporting APD (i.e. 3D; 3.5D, SiP, Photonics etc.
- Design supported by Signal Integrity and Thermal simulation

Thermal Engineering



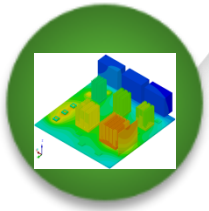
Ensure Product Thermal Integrity

- Analyze product thermal performance from chip to system
- Design thermal solutions for all reference and turn-key systems
- Evaluate device thermal runaway risk



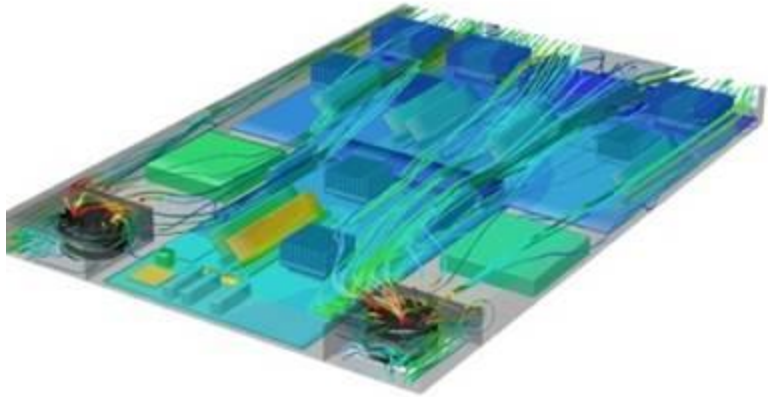
Enable Customer Thermal Design

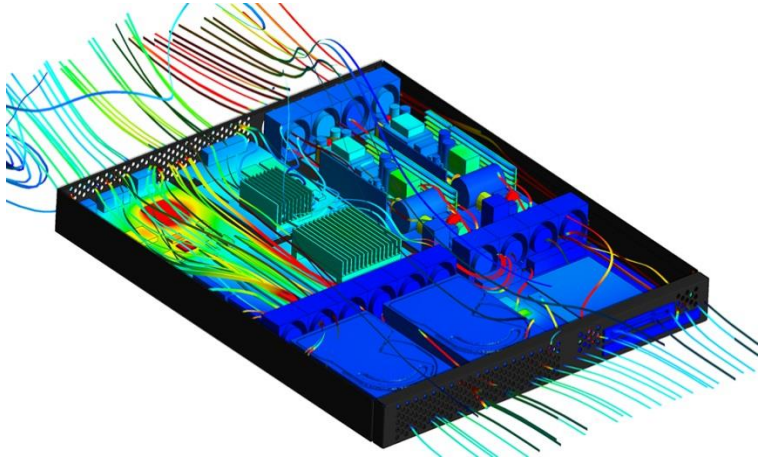
- Deliver thermal models to enable customer thermal design
- Help customers resolve thermal issues



Enhance Product Thermal Performance

- Evaluate new product thermal materials
- Improve thermal performance of new package technologies



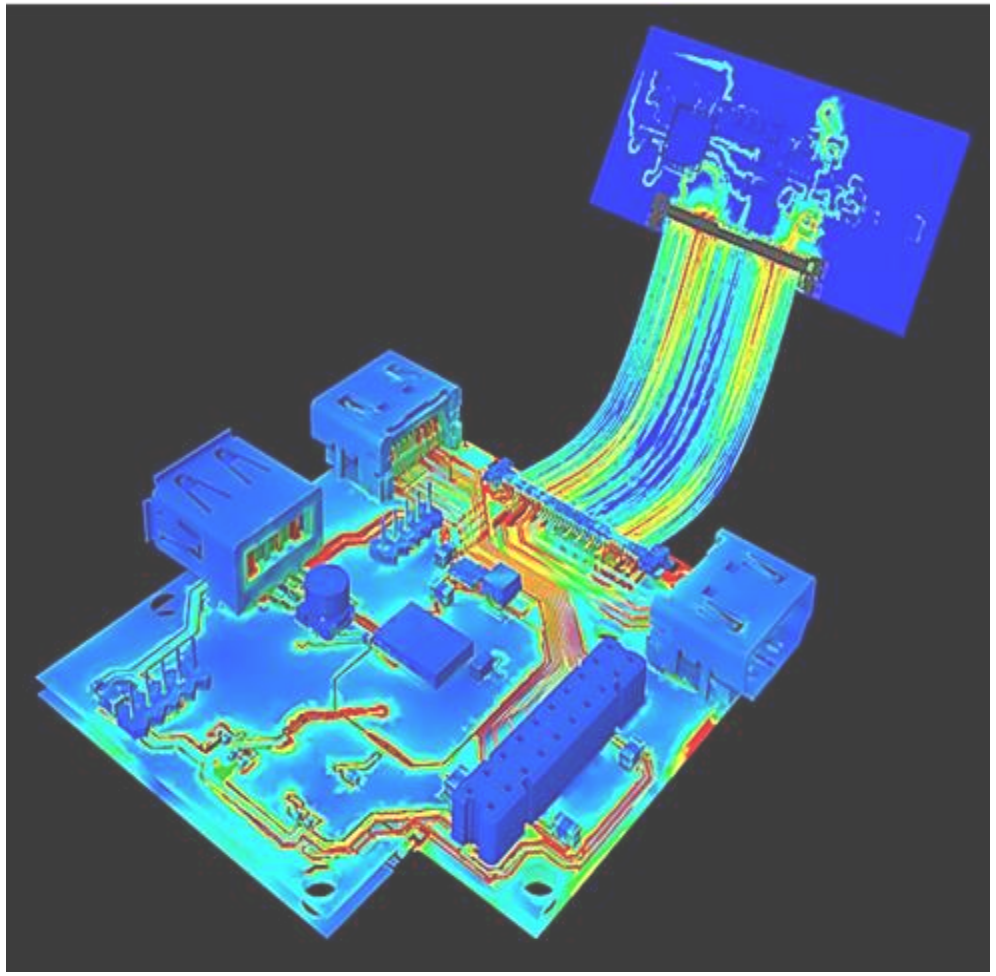


Signal Integrity

Die-Package-System Co-Design & Optimization for High Volume Manufacturing

SI / PI / EMI
Capabilities

Package design supported by electrical simulation for optimized performance



Package design workflow

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Package Development Workflow From Design Concept to High Volume Manufacturing

Project Kick-off	Package, Supplier Selection, & Pricing	Package Design & Development	Design Review and Finalization	Design Tape Out	Sample Bring Up and Package Qualification	Pre-Production & Optimization before HVM
• Chip specifications • SI requirement • Thermal requirement • Tape out schedule • Production ramp-up timeline • Cost budget	• Technology Availability • Supplier Tooling & Capacity Availability • Cost Analysis	• Die floor plan • Bump / bond-pad assignment and BGA ball assignment • Design Rule and layer stack-up • Supplier manufacturability	• Thermal Simulation & Validation • Stress Simulation & Validation • SI Simulation & Validation • Digital and analog IP review and approval	• Pre-tape out checklist for die and package tape out • Netlist release in PLM • MOD and POD release in PLM	• Assembly instruction for engineering prototype and customer sampling builds • Package and board level reliability qualification	• Pilot lot run in supplier for Pre-Production & process Optimization • Product in production

Quality/Reliability

Scope/Responsibilities

- Device qualification & reliability assessment
- Manage all quality and reliability aspects of products
- Management of quality excursion
- Material disposition
- Supplier quality management
- Customer quality interface
- Process change management
- Quality control system management
- Document control

Supply Chain

Scope/Responsibilities

- Demand assessment & planning for production and engineering builds
- Inventory management
- Capacity analysis
- Logistics & Warehouse management
- Maintain supplier relationship
- Import/Export compliance
- E&O
- Qtr end reporting

OPS ENGINEERING

Leveraging for your
10x Business Performance

- **Package Engineering - Ready**
  - Package design
  - Development
  - Signal Integrity, EM
  - Thermo/Mechanical CHAR
  - Assembly Process CHAR
  - Qualification
- **Test Engineering - In Development**
  - Test program development.
  - HW design
- **Product Engineering - Ready**
  - Device Qual
  - Product CHAR
  - Foundry Interface
- **Foundry Process Engineering & Device Physics - Ready**
- **Supply Chain, Sourcing and Planning - Ready**
- **Quality and Reliability - Ready**

Embedded and firmware Capabilities

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Chipsets and Hardware	OS and Middleware	Device Drivers and Firmware	Boot Software	Hardware Bring-up & Validation	Hardware Integration System
Integrated Product Design and Maintenance Services					
Embedded Platform Software Service					
Embedded Platform Migration Service					
Systems Integration Service					
• ARM • TI • Intel • Qualcomm • STMicro • NXP/Freescale	• OS Porting • Migration of Application and Product • Middleware Development, Customization • Testing	• Device Drivers • BSP Development • Core , I/O, Storage , multimedia and communication • Firmware development and validation	• Boot-Loader, BIOS • Customization enhancement & validation • OS boot including secure boot • OS firmware updates	• Pre and post silicon validation • Diagnostics @ Board & system levels [not clear] • Board bringing-up	• Board design • FPGA design

Data Protection

Network Access

- Firewall
- IP protection
- Port protection
- Authorized domain uses
- Password protection
- VPN
- Hard token based on customer demand

Device (Laptop/Mobile)

- Monitoring user access in office devices
- Fishing/Spying monitoring
- Allowed only registered software

Office premises

- Security check for employee
- Protected work zone
- a. Protected area
- b. Green zone
- Restricted to take personal device in protected area

File protection

- Prohibited Copy/ Paste/ Screen Save to external device
- File access authorization and permission

Email protection

- Encrypted facility
- Attachment protection

Meeting protection

- MS Teams
- Restricted for external user

Protection for customer IP file

- Engineer/Active and Service level Agency (SLA)
- Same engineer does not allow on different customer protection

Confidentiality Agreement/NDA

- Obligates of receiving party to protect that disclosing party's confidential information from tertiary events
- Allows disclosure of confidential product from the receiving party, only on a “need to know” basis

COMMITMENTS

- Customer Data Confidentiality
- IP protection
- Clear communication and language proficiency
- Resource backup
- Transparency
- Competitive pricing
- Dedicated resources, ensuring that assigned engineers are fully committed to the client’s project and are not involved in other assignments.

THANK YOU

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